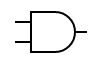
**LAB#08**

**OBJECT: Construct a truth table for y = where x is 3-bit input variable. Design a k.map for the truth table, minimize it and design circuit for minimize expression.**

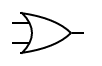
**APPARATUS:**

* 74LS08
* 74LS04
* 74LS32
* 74LS86
* Bread Board
* Connecting Wires
* LED
* DC Supply

**SYMBOLS:**



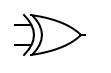
AND GATE



OR GATE



NOT GATE



XOR GATE

**TRUTH TABLE:**

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **X** | **A** | **B** | **C** | **Y0** | **Y1** | **Y2** | **Y3** | **Y4** | **Y5** | **Y** |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 |
| 2 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 4 |
| 3 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 9 |
| 4 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 16 |
| 5 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 25 |
| 6 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 36 |
| 7 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 49 |

**KARNAUGH MAP:**

K-MAP FOR Y0:

|  |  |  |
| --- | --- | --- |
|  |  |  |
|  | 0 | 0 |
|  | 0 | 0 |
|  | 1 | 1 |
|  | 0 | 0 |

**Y0= AB**

K-MAP FOR Y1:

|  |  |  |
| --- | --- | --- |
|  |  |  |
|  | 0 | 0 |
|  | 0 | 0 |
|  | 0 | 1 |
|  | 1 | 1 |

**Y1= AC + A = A(C+)**

K-MAP FOR Y2:

|  |  |  |
| --- | --- | --- |
|  |  |  |
|  | 0 | 0 |
|  | 0 | 1 |
|  | 0 | 0 |
|  | 0 | 1 |

**Y2= BC + AC = C(B + A) = C(A⊕B)**

K-MAP FOR Y3:

|  |  |  |
| --- | --- | --- |
|  |  |  |
|  | 0 | 0 |
|  | 1 | 0 |
|  | 1 | 0 |
|  | 0 | 0 |

**Y3= B**

K-MAP FOR Y4:

|  |  |  |
| --- | --- | --- |
|  |  |  |
|  | 0 | 0 |
|  | 0 | 0 |
|  | 0 | 0 |
|  | 0 | 0 |

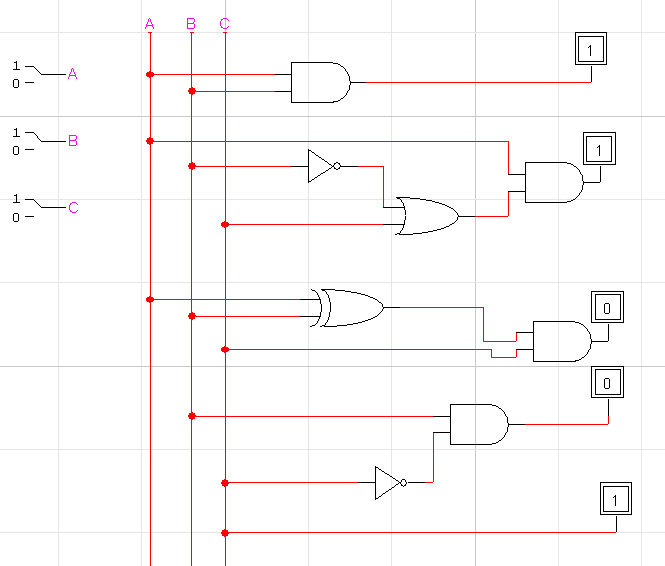
**Y4=0**

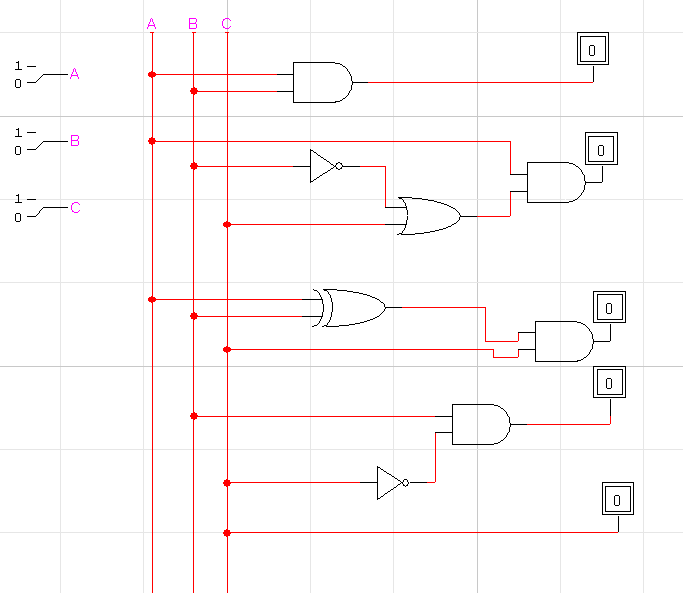
K-MAP FOR Y5:

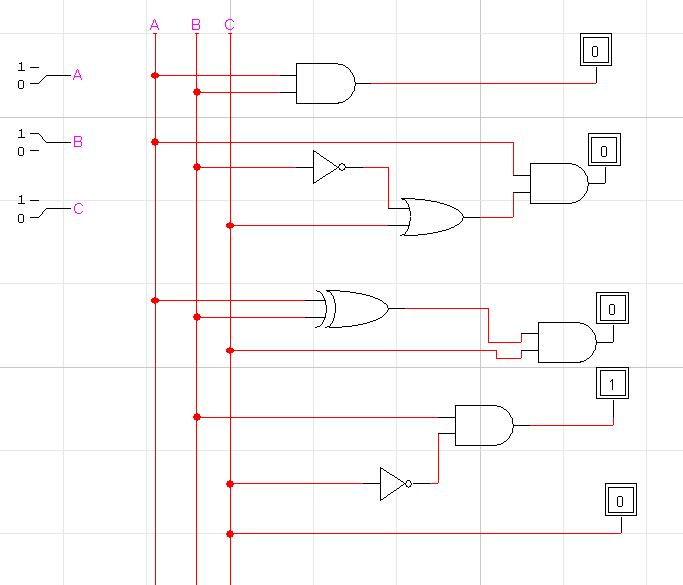
|  |  |  |
| --- | --- | --- |
|  |  |  |
|  | 0 | 1 |
|  | 0 | 1 |
|  | 0 | 1 |
|  | 0 | 1 |

**Y5= C**

**CIRCUIT DESIGN:**







**CONCLUSION:**

The circuit is working according to the truth table.